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(54) INTELLIGIBLE CROSSTALK PROTECTIVE SYSTEM FOR TIME DIVISION SWITCHING CENTRES

(71) We, INTERNATIONAL STANDARD ELECTRIC CORPORATION, a Corporation organised and existing under the Laws of the State of Delaware, United States of America, of 320 Park Avenue, New York 22, State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a crosstalk protective system for time division switching centres using pulse code modulation, especially to telephone exchanges.

In such a centre, the speech signals from subscriber's lines are sampled at 8kHz and each sample is converted by a coder into a coded combination of 8 bits including a bit indicating the polarity and 7 bits defining the amplitude of the sample. The combinations from 32 lines, for instance, are sent to a multiplexor which produces a series primary multiplex group. Within a multiplex cycle of 125 μs, corresponding to the repetition period of the combinations of a line, the multiplexor transmits serially the 32 combinations from the 32 lines, at the rate of a bit about every 500 ns. A supermultiplexor can then combine 8 primary multiplex groups, for instance, to constitute a secondary multiplex group. Within a multiplex cycle of 125μs, the secondary group routes the 256 combinations from the 8 primary groups. The combinations from the same line are thus sent within the time intervals of about 500 ns repeated every 125 μs and constituting a time channel. These combinations are sent either serially on a conductor at the rate of a bit about every 60 ns, or in parallel on 8 conductors, one per bit.

In the other transmission direction, from a secondary multiplex group routing the signals for 256 lines, a superdemultiplexor first separates the 8 primary multiplex groups, and for each of them, a demultiplexor provides for 32 lines, coded combinations which are decoded, restoring after a filtering operation, the speech signals.

As there are several incoming and outgoing secondary multiplex groups, calls are set up with a switching network which selects the combinations on a time channel of an incoming secondary group (corresponding to a calling line, for instance) and routes them to a time channel of an outgoing secondary group (called line, for instance). A similar path is simultaneously set up for the other direction (called line towards calling line).

The switching network effects space switching operations (connections from one group to another group); and time switching operations (connections from one channel to another channel); it includes, for that purpose, space switches and memories. This network can be, for instance, of the so-called space-time-space type. A connection path between an incoming channel of a first line (A) and an outgoing channel of a second line (B) goes through two switches arranged one on each side of a memory cell; one of them enables it to have access to the incoming secondary multiplex groups, the other one to the outgoing secondary multiplex groups. In this way, within each multiplex group, at the channel time for the incoming channel (line A) and through the first switch directed towards the appropriate incoming group, a combination from this incoming channel is registered in the memory cell. At the channel time for the outgoing channel (line B) and through the second switch directed towards the appropriate outgoing group, the combination from the incoming channel and kept in the memory cell is retransmitted onto this outgoing

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channel. The connection in the opposite direction, between the incoming channel of the second line (B) and the outgoing channel of the first line (A) is set up in the same way.

In practice the numerous necessary memory cells are memory cells belonging to several speech memories, and two space switches are associated with each of these memories. At each channel time, a memory cell is connected by the switches to the appropriate incoming and outging groups. In such a centre, the supermultiplexors, switches, memories, superdemultiplexors are units which process, through time-division multiplexing, a great number of calls. Every failure in these units seriously degrades the service of the whole centre and means for palliating the effects of failure are thus important.

One of the faults which can occur in these units, e.g. due to a failure in the addressing circuits, results in the parallel connection of two incoming channels, towards the same outgoing channel. Due to the short-circuit of a component a switch can thus associate the input of a memory, not only with a specified incoming secondary multiplex group, but also with another incoming multiplex group. The coded combinations originating from these two groups will then be mixed up. Such a fault can affect all the calls processed by the considered switch. It is consequently important to minimize its effects.

The parallel connection of two channels generally results in the combination, in "OR" manner of the combinations from two channels. If the nominal incoming channel is silent, the corresponding outgoing cannel will receive the combinations from the disturbing incoming channel. This constitutes a sort of intelligible crosstalk which cannot be accepted.

The present invention concerns a crosstalk protective system in time division switching centres which minimizes the effects of an accidental parallel connection of two incoming channels.

According to the invention, there is provided a time division multiplex switching centre wherein intelligence is conveyed by pulse code modulation combinations each including a sign bit and a number of amplitude-representing bits, in which to protect against intelligible crosstalk code conversion means are inserted at or near the inputs of the centre, in which each said code conversion means inverts some or all of the amplitude-representing bits of a combination when the sign bit thereof has one of its two possible values but does not invert when that sign bit has the other of its two possible values, in which said code conversions means does not invert the sign bits of the code combinations, in which complementary code conversion means are located at or near the outputs of the centre, and in which the output code conversion means inverts the same bits of the code combinations as did the input code conversion means when, and only when, the sign bit of the combination has that one value, so that when one channel is silent, i.e. its combination represents a null or almost null value, then a multiple connection which causes that combination to be added to another combination always produces an unintelligible result.

According to the invention there is also provided a time division multiplex switching centre wherein intelligence is conveyed by pulse code modulation combinations each including a sign bit and a number of amplitude-representing bits, in which at or near the inputs of the centre code conversion means is provided which inverts the amplitude representing bits of a code combination whose sign bit has one prescribed value but does not invert the amplitude-representing bits of a combination whose sign bit has the other value, and in which at the outputs of the centre code conversion means are provided to produce similar inversions to those produced at the inputs, whereby if a multiple connection occurs, intelligible crosstalk is obviated.

An embodiment of the invention will now be described in conjunction with the drawing, wherein figure 1, is a block diagram of a time division switching centre and figure 2, is a code conversion used in the centre of figure 1.

In figure 1, incoming lines le_0, le_1 . . ., le_{31}, are connected to a multiplexor M_0 which associates them to constitute an incoming primary multiplex group gpe_0. These incoming lines provide the multiplexor with the 8-bit coded combinations each including a polarity bit and 7 amplitude bits, which is represented by the expression S abcdefg. Each incoming line provides a combination every 125 μs. Within a cycle of 125 μs, the multiplexor M_0 provides, on the primary group gpe_0, serially the 32 8-bit combinations from the lines le_0 to le_{31} at the rate of a bit about every 500 ns. Other multiplexors (not shown) constitute in the same way incoming primary groups gpe_1 to gpe_7.

The function and the constitution of the code conversion devices such as T*e* in the incoming primary groups will be described later.

The incoming primary groups gpe_0 to gpe_7 are connected to a supermultiplexor SM_0 which associates them to constitute an incoming secondary multiplex group gse_0. This secondary group is of the "parallel" type, and has as many conductors as a

coded combination comprises bits, i.e. 8. Within a cycle of 125μs, the supermultiplexor SM_0 thus provides on the secondary group gse_0, in parallel, the (8 × 32) combinations from the primary groups gpe_0 to gpe_7, at the rate of a combination about every 500 ns. Other supermultiplexors (not shown) constitute in the same incoming secondary groups gse_1 to gse_n.

All the incoming secondary groups are connected to a connection network RC controlled by a control unit UC. Outgoing secondary groups gss_0, $gss_1 \ldots gss_n$ similar to the incoming groups, are also connected to this network. The network RC and its control unit can take on different forms and are outside the scope of the invention, and are not described herein.

The outgoing secondary multiplex group gss_0 leads to the superdemultiplexor SD_0 which separates it into 8 outgoing primary multiplex groups gps_0, $gps_1 \ldots gps_7$. The signals conveyed by these outgoing primary groups are the same as those of the incoming primary groups. Other superdemultiplexors (not shown) decompose in the same way the outgoing secondary multiplex groups gss_1 to gss_n.

The outgoing primary multiplex group gps_0 leads to the demultiplexor D_0 which distributes the 32 combinations it receives within each multiplex cycle on 32 outgoing lines $ls_0, ls_1 \ldots ls_{31}$.

The function and the constitution of the code conversion devices such as T*s* in the outgoing primary groups will be described later.

An incoming line le_0 associated with an outgoing line ls_0, for instance, corresponds in figure 1 to each subscriber's line. The subscriber's line and the equipment, hybrid circuit, coder and decoder, individual to it and connecting it to the incoming and outgoing lines are not shown. To an incoming line (le_0) there then corresponds a time channel in a primary group (gpe_0) then a time channel in a secondary group (gse_0). Similarly a time channel of a secondary group (gss_0) and a time channel of a primary group (gps_0) correspond to an outgoing line (ls_0).

Every telephone call needs the connection of the caller's incoming line to the called line's outgoing line, and the connection of the called line's incoming line to the caller's outgoing line. The switching network RC, to set up such a call, routes the combinations it receives on a time channel of an incoming secondary group (corresponding to the caller's incoming line) to a time channel of an outgoing secondary group (corresponding to the called line's outgoing line). A similar connection is simultaneously set up between another time channel of an incoming secondary group (incoming line of the called line) and another time channel of an outgoing secondary group (outgoing line of the calling line).

All the required calls are thus set up in the network RC in response to orders from the central unit UC.

The invention relates in particular to failures whose effect of which is such that combinations from two incoming lines (le_0 and le_1, for instance) are sent simultaneously to an outgoing line (ls_{31}, for instance), while this outgoing line ls_{31} should receive only the combinations from the incoming line le_0; such a failure can occur in any one of the units on the path of these combinations, e.g. in the switching network RC.

Without protective devices, the combinations from two incoming lines will be superposed in a general way, according the logic function "OR". If one combination is 1 1100011 and the other 0 1101101, the outgoing line receives 1 1101111. There is no addition of the coded signals from the two lines and, although the call between the lines le_0 and ls_{31} is disturbed, the result of the superposition is such that the voice signals from the line le_1 will not be perceived in an intelligible way by the subscriber of the line ls_{31}. However, if the subscriber of the line le_0 remains silent, the combinations on the incoming line le_0 will be of the type 0 0000000 or 1 0000000. Particularly, in the case of the combination 0 0000000, the superposition of any combination of the shape S abcdefg from the incoming line le_1 will provide this combination S abcdefg on the outgoing line ls_{31}. The subscriber of the line ls_{31} will thus hear distinctly the words pronounced by the subscriber of the line le_1 and which are not meant for him. Such intelligible crosstalk cannot be accepted.

To avoid this, code conversion devices T*e* and T*s*, are inserted into the transmission path of the coded signals to modify the combinations so that the failure previously considered cannot give rise to intelligible crosstalk. The device T*e* modifies the combinations and the device T*s* gives to them a complementary modification which cancels the first one, so that the combinations introduced at its inputs are found again unchanged. These code conversion devices have been inserted into the primary multiplex groups so that the protection includes the supermultiplexors, the switching network and the supermultiplexors, without, however, their number being excessive. Nevertheless, it is obvious that they could be arranged somewhere else either at the line levels, or at the secondary group level.

These code conversion devices T*e* and T*s* can be identical, as will be seen from figure 2.

The code conversion device of figure 2

includes a bistable circuit *cb*, two inverters *ih* and *iv*, "AND" gates *p*0 to *p*4 and "OR" gates *p*5 and *p*6. It receives on its input *ent* the combinations sent serially by a multiplexor such as M_0. It also receives, provided by clock means (not shown) a clock signal HO which coincides with the sign bit, i.e. the first bit of each combination. It finally provides on its output *st* modified combinations.

The operation will be described by assuming first that it receives, at *ent*, the first bit of a combination. We first assume that this bit is a 1. At the same time, the device receives the clock signal HO. Thus the "AND" gate *p*1 operates and provides a signal of value 1 which is directly retransmited on the output *st*, through the "OR" gate *p*6.

The output signal of the gate *p*1 is also applied to the bistable circuit *cb*, and sets it to 1. The bistable circuit then provides on its upper output a signal which makes conducting the gate *p*3. The input signal can pass through the gates *p*3 and *p*5, but is still blocked by the gate *p*4.

This first sign bit transmitted without any modification through the code conversion device up to the output *st* is followed by 7 amplitude bits. As the clock signal HO is completed, the inverter *ih* then provides a signal to open the gate *p*4, so the 7 amplitude bits follow a path in the code conversion device between the input *ent* and the output *st*, through the gate *p*3, the "OR" gate *p*5, the gate *p*4 and the "OR" gate *p*6. These bits are thus retransmitted onto the output *st* without modification.

Thus the code conversion device does not modify the combinations the sign bit of which is 1.

We now assume that a combination whose sign bit is 0 occurs. The clock signal HO is provided simultaneously with this sign bit. As the latter has a value 0, the gate *p*1 does not operate, while the inverter *iv* provides a signal of value 1. The gate *p*0 operates and provides a signal to reset the bistable circuit *cb*, which then opens the gate *p*2. The gate *p*4 is blocked by the inverter *ih*, and no signal is provided on the output *st*, which corresponds to the transmission of a sign bit of value 0. The sign bit is thus transmitted, again without any modification.

The 7 amplitude bits then follow. As the signal HO is completed, the gate *p*4 is made conducting. The 7 bits find in the code conversion device a path through the inverter *iv*, the gate *p*2, the gate *p*5, the gate *p*4, the gate *p*6. This path includes the inverter *iv*, so the bits transmitted to the output *st* are inverted in relation to those received on the input *ent*.

Thus it will be seen that the code conversion device transmits without modification the combinations whose sign bit is value 1, while combinations whose sign bit is 0 have their amplitude bits inverted.

It operates serially as it is at the level of the primary groups. Clearly designing a parallel device performing the same code conversion at the level of the secondary groups would offer no difficulty.

The interposition of two similar devices (T*e* and T*s*) in the transmission path for the combinations brings to some combinations two successive inversions which cancel each other, so that, in the centre of figure 1, the combinations provided by the incoming lines are found again on the outgoing lines. The devices T*e* and T*s* of figure 1 can be identical with the device of Figure 2.

The effect of the protecting device will now be considered when failure occurs, and particularly when the channel normally through-connected being silent, the disturbing channel would be liable to be distinctly heard. As before, the case of a failure will be assumed in the switching network RC (Figure 1) which brings a mixing of the combinations from lines le_0 and $1e_1$ towards line $1s_n$.

The critical case, as already indicated, is when the incoming line normally through-connected is silent, i.e. provides combinations which can be, at random, either of the type 0 0000000, or of the type 1 0000000. The device T*e* converts the first combination into 0 1111111. while 1 0000000 remains unchanged. The mixing of 0 1111111 with any combination S abcdefg, provides a combination S 1111111. Then, according to the value of S, the code conversion device T*s* will provide, towards the outgoing line ls_n, either the combination 1 1111111, or the combination 0 0000000. The disturbing signal thus produces no crosstalk.

If the mixing of the combination 1 0000000 with any combination S abcdefg, is considered, the result is 1 abcdefg; this is transmitted without modification by T*s* towards the outgoing line ls_n. This modification of the sign suffices, as will be seen, to make the disturbing signals unintelligible. Indeed, the disturbing combination, if it initially had its sign S equal to 0, was inverted in the input-side code conversion device (T*e* in the case of crosstalk previously considered), so this inversion is not cancelled by T*s*, as the sign has become 1 in the combination due to the mixing. Consequently, the signals reaching the outgoing line $1s_n$ will be inverted whenever the original sign is 0, so that the sign is simultaneously inverted and the resulting voice signal made unintelligible.

Of course, if the incoming line le_0 provides non-null combinations, because the

subscriber speaks,. these combinations will be combined without being added to the disturbing combinations and those will not give rise to an intelligible crosstalk.

Such an arrangement, wherein code conversion devices such as shown in Figure 2 are inserted into the centre, enable at little cost, the elimination of any risk of intelligible crosstalk by mixing two channels in a time division switching centre.

WHAT WE CLAIM IS: —

1. A time division multiplex switching centre wherein intelligence is conveyed by pulse code modulation combinations each including a sign bit and a number of amplitude-representing bits, in which to protect against intelligible crosstalk code conversion means are inserted at or near the inputs of the centre, in which each said code conversion means inverts some or all of the amplitude-representing bits of a combination when the sign bit thereof has one of its two possible values but does not invert when that sign bit has the other of its two possible values, in which said code conversions means does not invert the sign bits of the code combinations, in which complementary code conversion means are located at or near the outputs of the centre, and in which the output code conversion means inverts the same bits of the code combinations as did the input code conversion means when, and only when, the sign bit of the combination has that one value, so that when one channel is silent, i.e. its combination represents a null or almost null value, then a multiple connection which causes that combination to be added to another combination always produces a unintelligible result.

2. A switching centre as claimed in claim 1, and in which each said code conversion means includes a bistable circuit set to one or the other of its two states according to the value of the sign bit of each code combination, and two transmission paths in parallel and conditioned respectively by the two complementary outputs of the bistable circuits, one of the two paths routing the amplitude-representing bits of the combinations without inverting them, while the other includes an inverter which when its path is conditioned inverts those bits.

3. A switching centre as claimed in claim 1 or 2, in which a number of incoming primary multiplex groups are supermultiplexed into a plurality of supermultiplex groups, in which the input code conversion means are each inserted into one of the primary multiplex groups, in which each of the supermultiplex groups is superdemultiplexed into its constituent outgoing primary multiplex groups, and in which the output code conversion means are each inserted into one of the outgoing primary multiplex groups.

4. A time division multiplex switching centre wherein intelligence is conveyed by pulse code modulation combinations each including a sign bit and a number of amplitude-representing bits, in which at or near the inputs of the centre code conversion means is provided which inverts the amplitude representing bits of a code combination whose sign bit has one prescribed value but does not invert the amplitude-representing bits of a combination whose sign bit has the other value, and in which at the outputs of the centre code conversion means are provided to produce similar inversions to those produced at the inputs, whereby if a multiple connection occurs, intelligible crosstalk is obviated.

5. A time division multiplex switching centre, substantially as described with reference to the accompanying drawings.

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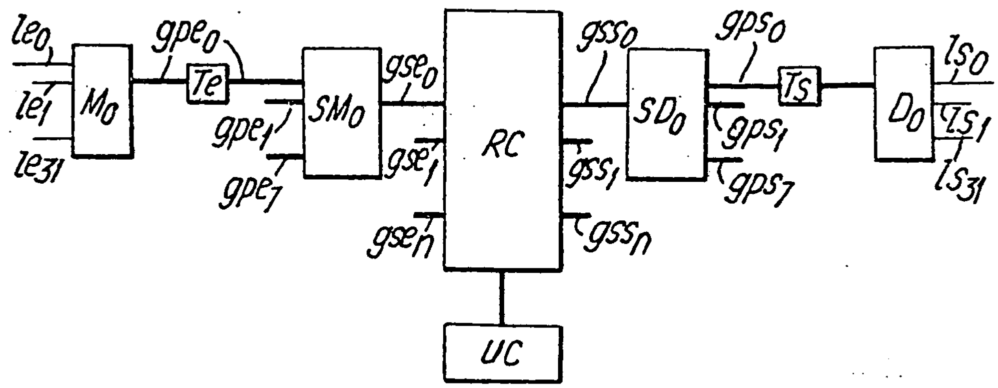
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Fig. 1.

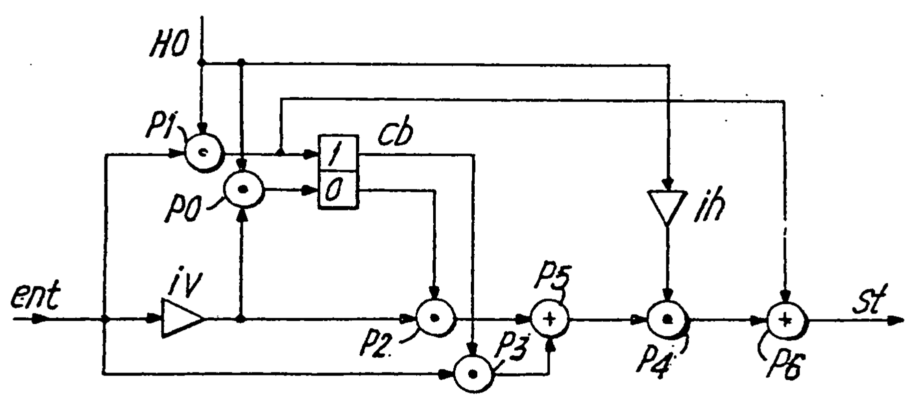
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Fig. 2.

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